REMARKS

Claims 1-7 are pending in the application. Claims 1, 2, 6 and 7 have been rejected under 35 USC 103(a) as being unpatentable over Settle in view of Tsubouchi; and Claims 3-5 have been rejected as unpatentable over Settle and Tsubouchi and further in view of Yamauchi. For the reasons set forth below, Applicants believe that the claims are patentable over the cited art.

The present invention provides a format conversion circuit for conversion of video data comprising lines of data with horizontal synchronizing periods between adjacent lines of video data. The circuit comprises a memory for storing video data; a header generation device for generating a packet header that adheres to a standard for motion picture compression; a synchronous timing detector for detecting a synchronizing signal at the start of a line of data; and a selection device for repeating the selection of the packet header generated by said header generation means and selection of a predetermined amount of video data read out of said memory as a payload responsive to the packet header, during an interval from when said synchronous timing detection device detects the synchronizing signal for a line until it detects the next

synchronizing signal for the next successive line. Under the present invention, the alternate selection of header data and video data for the payload continues until all of the data for the line of video data has been placed in packets. Given the additional time required to insert the packet headers, the present invention takes advantage of the horizontal synchronizing period after each line of data and before a next successive line of data (i.e., before the next detected synchronizing signal) to complete packetizing the data for the line, whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data. The format conversion system can use the clock of the input video signal as the clock for reading out the data (i.e., packetizing the data). The format conversion method and program storage device are additionally taught and claimed.

Applicants have amended the language of the independent claims to expressly recite that the video data comprises lines of data and horizontal synchronizing periods (see, e.g.: Fig. 6; page 9, lines 21-29; page 11, lines 4-8) and that the selecting of video data continues into the horizontal synchronizing period (see: e.g., page 9, line 30-page 10, line 4; Figs. 7, 9 and 10; and page 16, lines 21-25). Support for the amendment language is

clearly found in the Specification. Applicants respectfully assert that the claims, as amended, are patentable over the cited art.

The Settle patent provides teachings regarding generating a packet header. The Examiner has acknowledged that Settle does not disclose the storing of unpacketized data in a memory, the detecting of a synchronizing signal, or the selection of a predetermined amount of video data read out of the memory as a payload responsive to the packet header during an interval between synchronizing signals. The Examiner has cited the Tsubouchi patent as providing the teachings which are missing from the Settle patent.

The Tsubouchi reference is directed to a system for displaying requested video content with minimal delay. Tsubouchi provides a plurality or video devices that can deliver video content without going through the system bus. Tsubouchi minimizes delay by allowing the video devices to directly output the video content. Applicants acknowledge that Tsubouchi teaches that it is known to store video in a buffer and to read the video data out of the buffer in response to a signal. Tsubouchi does not, however, teach or suggest converting the format of video data from one formal (e.g., analog) to another format (e.g., digital).

Further, Tsubouchi does not teach or suggest that the input video data comprises a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data. Tsubouchi does not teach detecting a synchronization signal for a line of the video data and packetizing the video data by alternately generating a packet header and selecting a predetermined amount of the video data as a payload until all of the data from the line of video data is packetized. Moreover, Tsubouchi does not teach or suggest the foregoing packetizing during an interval between detection of a synchronization signal for the line of data and detection of a synchronization signal for a successive line of data whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data.

Applicants respectfully assert that neither Settle nor Tsubouchi teaches or suggests the claim feature of selection of a predetermined amount of video data during an interval between successively detected synchronizing signals. While Tsubouchi teaches releasing video in response to a signal, Tsubouchi does not teach or suggest releasing a predetermined amount of video during an interval between successive synchronizing signals.

Further, there is nothing in the teachings of either Settle or Tsubouchi to motivate one having skill in the art to modify Settle with a video buffer of Tsubouchi. Further, even if one were to modify Settle with a video buffer, one would not arrive at the subject invention since neither reference teaches or suggests the detection of successive synchronizing signals and the selection of a predetermined amount of video data between the detected signals.

For a determination of obviousness, the prior art must teach or suggest all of the claim limitations. "All words in a claim must be considered in judging the patentability of that claim against the prior art" (*In re Wilson*, 424 F. 2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970). Since the cited references fail to teach each and every one of the claim limitations, a *prima facie* case of obviousness has not been established by the Examiner against Claims 1, 2, 6 and 7.

Applicants respectfully assert that the Examiner has also failed to establish a *prima facie* case of obviousness against the remaining claims. The primary reference against all claims is Settle. Applicants rely on the arguments set forth above with respect to the teachings of Settle, alone and in combination with the Tsubouchi reference. Applicants further assert that the additionally

cited references do not provide the teachings which are missing from the combination of Settle and Tsubouchi. The Yamauchi patent is cited for its teaching of producing a clock signal locked to the horizontal synchronization signal included in video input. The Examiner states that "it was known to sample video based on a horizontal synchronization signal". Applicants respectfully assert that, even if one were motivated to use a horizontal synchronization signal to sample video from the Settle system with a Tsubouchi video buffer, one would not arrive at the claimed invention since none of the references teaches or suggests the detection of successive synchronizing signals for lines of video data having horizontal synchronizing signals therebetween and the alternate generation of header data and selection of a predetermined amount of video data between the detected signals (Claim 3), with the counter counting and outputting a data valid signal (Claim 4) and a FIFO memory being reset in response to a data valid signal (Claim 5). Further, none of the cited references teaches erasing stored video data, as is expressly recited in Claim 5.

Based on the foregoing amendments and remarks, Applicants respectfully request entry of the amendment, reconsideration of the rejections, and issuance of the claims.

Respectfully submitted,

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